REMARKS

Claims 1-8 and 12-23 remain pending in the application.

The Applicants respectfully request the Examiner to reconsider earlier rejections in light of the following remarks. No new issues are raised nor is further search required as a result of the changes made herein. Entry of the Amendment is respectfully requested.

Claims 1-6, 17-19 and 22 over Persaud in view of Luan

Claims 1-6, 17-19 and 22 were rejected under 35 U.S.C. §103(a) as allegedly being obvious over Persaud et al., UK Patent Application No. GB2074762 ("Persaud") in view of Luan, U.S. Patent No. 5,911,149 ("Luan"). The Applicants respectfully traverse the rejection.

Claims 1-6, 17-19 and 22 recite a second agent receiving a clock signal from a first agent on a dedicated clock line.

The Examiner acknowledges that Persaud discloses synchronization signals applied over a backplane (Office Action, page 15). However, the Examiner alleges that a synchronization signal is synonymous to a clock signal and the routing of a signal does not prevent it from being a clock signal, with no evidence to support an assertion to the contrary (Office Action, page 15).

The burden of proof is on the Examiner to prove the Applicants' claimed are unpatentable and to provide prior art that discloses or suggests the claimed features. The burden of proof is **NOT** on the Applicants to prove what the prior art teaches when not disclosing the claimed features. The Applicants respectfully request that if the Examiner continues to maintain that Persaud's synchronization signals are clock signals, the Examiner provide support for such an allegation.

Persaud's synchronization signals are data signal, NOT interpreted as a clock signal even with a broadest interpretation of the claims. A clock signal is a **term of art** equating to an oscillating signal that is used to control timing within a circuit, carrying no information itself. A synchronization signal is a data signal that contains information used to instruct a circuit to perform a

synchronization operation. The Examiner has not provided any proof that Persuad is equating the disclosed synchronization signal to a clock signal, much less that Persaud's backplane even contains clock signals.

Moreover, to more clearly distinguish Applicants' claimed features with Persaud's disclosed use of synchronization signals transported over data lines, claims 1-6, 17-19 and 22 are amended herein to recite a clock signal on dedicated clock line. Since Persaud synchronization signal is a data signal, it would be transported on a data line with other data information. Persaud fails to disclose a second agent receiving a clock signal from a first agent on a dedicated clock line, as recited by claims 1-6, 17-19 and 22.

The Examiner acknowledges that Persaud fails to disclose use of synchronous memory (Office Action, page 4). However, the Examiner alleges that the fact that Persaud is old does not prevent such design from disclosing the claimed invention, but in fact goes to establish that Applicant's claimed features were known for a long time (Office Action, page 15). The Applicants respectfully disagree.

"Teachings of references can be combined only if there is some suggestion or incentive to do so." In re Fine, 5 USPQ2d 1596,1600 (Fed. Cir. 1988) (quoting ACS Hosp. Sys. v. Montefiore Hosp., 221 USPQ 929, 933 (Fed. Cir. 1984)) (emphasis in original). The Examiner acknowledged that Persaud fails to disclose synchronous memory. However, neither Persaud nor Luan provide any motivation to completely redesign Persaud's system to include a synchronous memory, which could not simply be dropped in to replace the disclosed asynchronous memory. The inclusion of synchronous memory would not alleviate any disclosed shortcomings in Persaud to provide any new functionality. In fact, completely redesigning Persaud's system to replace the disclose asynchronous memory with synchronous memory would result in Persaud still solving the same disclosed problem of sharing a memory between a master and slave. Persaud modified by Luan would still fail to address timing issues that are addressed by Applicants' clock routing.

The Office Action alleges that Luan is relied upon for teaching variably sized memory banks and it not relied on for teaching routing clock

signals (Office Action, page 15). However, as discussed above, "Teachings of references can be combined only if there is some suggestion or incentive to do so." In re Fine, 5 USPQ2d 1596,1600 (Fed. Cir. 1988) (quoting ACS Hosp. Sys. v. Montefiore Hosp., 221 USPQ 929, 933 (Fed. Cir. 1984)) (emphasis in original). The Examiner has not provided any motivation why one of ordinary skill in the art would have been motivated to modify Persaud with Luan alleged disclosure of variably sized memory banks. Persaud modified with variable sized memory banks would not alleviate any shortcomings in Persaud. In fact, modifying Persaud with variably sized memory banks would fail to add benefits to Persaud's basic function of sharing a common memory with both a master and slave.

Thus, Persaud modified by Luan, even if one of ordinary skill in the art were to combine the two references for some reason, would still fail to disclose or suggest a second agent receiving a clock signal from a first agent on a dedicated clock line, as recited by claims 1-6, 17-19 and 22.

Accordingly, for at least all the above reasons, claims 1-6, 17-19 and 22 are patentable over the prior art of record. It is therefore respectfully requested that the rejection be withdrawn.

Claims 7, 8, 12, 20, 21 and 23 over Wu in view of Persaud and Persaud in view of Wu

Claims 7, 8 and 12 were rejected under 35 U.S.C. §103(a) as allegedly being obvious over Wu et al., U.S. Patent No. 5,659,715 ("Wu") in view of Persaud; claims 20 and 21 rejected under 35 U.S.C. §103(a) as allegedly being obvious over Persaud in view of Wu; and claim 23 was rejected under 35 U.S.C. §103(a) as allegedly being obvious over Wu. The Applicants respectfully traverse the rejection.

Claims 7, 8, 12, 20, 21 and 23 recite a second agent receiving a clock signal from a first agent on a dedicated clock line.

As discussed above, Persaud fails to disclose or suggest a second agent receiving a clock signal from a first agent on a dedicated clock line, as recited by claims 7,8, 12, 20, 21 and 23.

Wu appears to disclose a first and second processor having access to a common memory bank (Fig. 3, items 302, 400 and 304 respectively). Address and data lines (Wu, items 306 and 308) running to the common memory bank (Wu, item 304) are routed through a single source, the graphics controller (Wu, item 400). The CPU (item 302) and the graphics controller are tied together to route data to the common memory (Wu, Fig. 3). The common memory is connected to the graphics controller which is connected to the CPU (WU, Fig. 3). A clock synthesizer interface provides for programming of a programmable clock synthesizer (Wu, col. 8, lines 39-43).

Wu discloses a system in which a CPU and a graphics controller utilize a common clock signal produced by a programmable clock synthesizer to access a common synchronous memory. Although Wu discloses two agents accessing a common synchronous memory, Wu does NOT disclose or suggest a second agent receiving a clock signal from a first agent on a dedicated clock line, as recited by claims 7, 8, 12, 20, 21 and 23.

Neither Wu modified by the teachings of Persaud nor Persaud modified by the teachings of Wu disclose, teach or suggest a second agent receiving a clock signal from a first agent on a dedicated clock line, as recited by claims 7, 8, 12, 20, 21 and 23.

At best, even if the combination of Wu and Persaud were obvious, which it is not, the theoretical combination would result in a system and method of using a CPU and graphics controller for accessing a common memory. A programmable clock synthesizer would provide a clock signal to ALL the CPU, graphics controller and memory within the system. The CPU would additionally send synchronization data signals to the graphics controller, which would be nonsensical since the graphics controller is already receiving a clock signal. Thus, even the theoretical combination fails to disclose or suggest a second agent receiving a clock signal from a first agent on a dedicated clock line, as recited by claims 7, 8, 12, 20, 21 and 23.

Accordingly, for at least all the above reasons, claims 7, 8, 12, 20, 21 and 23 are patentable over the prior art of record. It is therefore respectfully requested that the rejection be withdrawn.

Claims 13-16 over Persaud in view of Muthal

Claims 13-16 were rejected under 35 U.S.C. §103(a) as allegedly being obvious over Persaud in view of Muthal, U.S. Patent No. 5,815,167 ("Muthal"). The Applicants respectfully traverse the rejection.

Claims 13-16 recite a second agent receiving a clock signal from a first agent on a dedicated clock line.

As discussed above, Persaud fails to disclose or suggest a second agent receiving a clock signal from a first agent on a dedicated clock line, as recited by claims 13-16.

The Office Action relies on Muthal to allegedly make up for the deficiencies in Persaud to arrive at the claimed invention.

Muthal appears to disclose a computer system comprising a graphics controller, a memory controller and shared memory (Abstract). The shared memory is accessible by both the memory controller and graphics controller (Muthal, Abstract). Concurrent access to portions of the shared memory is given to the graphics controller and the memory controller (Muthal, Abstract).

Although Muthal discloses a first and second agent accessing different portions of a shared non-dedicted memory memory simultaneously, Muthal fails to disclose how access to the shared portion of the memory system is synchronized between the processor and the graphics controller. Muthal makes **no mention** of how clock signals are routed throughout the system, much less disclose or suggest a second agent receiving a clock signal from a first agent on a dedicated clock line, as recited by claims 13-16.

Thus, Persaud modified by the teachings of Muthal fails to disclose, teach or suggest a second agent receiving a clock signal from a first agent on a dedicated clock line, as recited by claims 13-16.

Accordingly, for at least all the above reasons, claims 13-16 are patentable over the prior art of record. It is therefore respectfully requested that the rejection be withdrawn.

Conclusion

All objections and rejections having been addressed, it is respectfully submitted that the subject application is in condition for allowance and a Notice to that effect is earnestly solicited.

Respectfully submitted,

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